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REMARKS

Claims 1, 3-18, 20-32 and 39 are currently pending in the above-identified application. Claims 1-32 have been rejected. The specification and claims 1, 9, 17, 18 and 26 have been amended. Claims 33-38, previously withdrawn from consideration, have been canceled along with claims 2 and 19 solely to further the prosecution of the above-identified application. New claim 39 has been added. No new matter has been added and new claim 39 is fully consistent with the specification as originally filed. Applicant respectfully reserves the right to reclaim the subject matter of the canceled and preamendment claims in this or any other application. Applicant respectfully requests reconsideration in light of the foregoing amendments and following remarks.

A Request for Drawings Change is being filed herewith, along with FIGS. 1-3. The changes to FIGS. 1-3, which is shown in red ink, are the inclusion of the legend PRIOR ART. Applicants respectfully request approval of the change to FIG. 1A.

Claims 17 and 26 stand rejected under 35 U.S.C. §112, first paragraph. Specifically, the Office action states there is no support in the specification for the recitation of "further comprising an array of said memory cells" in claim 17 and the recitation of "semiconductor die being electrically connected to said conductive connector" in claim 26.

As a threshold matter, the applicant wishes to direct the Examiner's attention to FIG. 8 in which a plurality of memory cells 513 are positioned in an array within the DRAM 512. The specification has been amended to indicate that the memory cells 513 are in an array. Further claim 17 has been amended to recite a plurality of memory cells, with a new dependent claim reciting that the plurality of memory cells are in an array.

Additionally, claim 26 has been amended by deleting the portion of the claim which the Office action alleges to be not supported by the specification.

Claims 11 and 25 stand rejected under 35 U.S.C. §112, second paragraph. The Office action states that the limitation "a conductive plug positioned within an insulator layer" lacks insufficient antecedent basis. Applicant respectfully traverses this rejection.

Applicant wishes to point out that the term "insulator layer" is preceded with the article "an", and not either "the" or "said", and therefore there should not be any antecedency issue as to that term. Furthermore, if "the scope of a claim would be reasonably ascertainable by those skilled in the art, then the claim is not indefinite." MPEP 2173.05(e). Applicant submits that claims 11 and 25 are sufficiently definite.

Claims 1, 3-8, 18, 20-21 and 23 stand rejected under 35 U.S.C. § 103(a) as being unpatentable over Hong et al. Applicants respectfully traverse this rejection.

Claim 1, as amended, recites a semiconductor structure that includes an insulator layer, a conductive plug, an etch-stop layer, a non-conductive layer, and a conductive connector formed in a via in electrical contact with the plug. The conductive connector includes a first conductive layer deposited in and in contact with the etched via and a second conductive layer deposited over the first conductive layer, the first conductive layer including a portion in contact with the conductive plug. Claims 3-8 depend from claim 1.

Claim 18, as amended, recites a semiconductor device with a conductive element, an etch-resistant layer, a non-conductive layer, a conductive material located in a via, and a doped region connected to the conductive element. Claims 20-21 and 23 depend from claim 18.

Hong et al. refers to a method of forming diffusion barriers encapsulating copper. In the background of Hong et al. is a discussion stating that diffusion barriers were known to be formed by etching a trench or via within a dielectric substrate and then depositing metallic compounds therein. Problems occurred through this technique, namely that the metallic compounds had numerous diffusion paths, due to their polycrystalline structure. Impurities were incorporated into the metallic compounds, which caused large increases in resistance-capacitance delay times. Thus, Hong et al. teaches away from "a first conductive layers deposited in and in contact with said etched via", as recited in claims 1 and 3-8, and from "a conductive material located in said via", as recited in claims 18, 20-21 and 23. Additionally, the wisdom in the industry at the time of the present invention was to utilize a timed etch process rather than provide a more expensive and more time intensive process to create an etch-stop layer. See U.S. patents numbers 6, 218,244; 6,114,218; 5,753,962; and 5,251,170.

With reference to claims 4-6, the Office action states that it would have been obvious to one of ordinary skill to form the etch-stop layer. As noted above, the wisdom in the industry was to perform a timed etch, not prepare an etch-stop layer. Applicant respectfully submits that, without a reference showing the use of an etch-stop layer with the recited semiconductor structure, the Examiner has failed to establish prima facie obviousness.

Further, Hong et al. fails to disclose or suggest "a doped region connected to said conductive element" as recited in claims 18, 20-21 and 23. Thus, one ordinarily skilled in the art would not have been motivated to utilize Hong et al. On one additional

note, the Office action seems to indicate that claim 1 is constrained to an etch-stop layer formed of silicon nitride. Applicant explicitly disagrees with that contention and notes that there is no recitation of silicon nitride in claim 1, but that such a recitation is found in a dependent claim thereof, namely claim 3.

Claims 2, 9-16, 19, 22 and 24-32 stand rejected under 35 U.S.C. §103(a) as being unpatentable over Hong et al. in view of FIG. 1 of the application. Applicant respectfully traverses this rejection as it applies to claims 9-16, 22 and 24-32.

Claims 9 and 10 are dependent from claim 1, and claims 22 and 24 depend from claim 18. Applicant has argued above that claims 1 and 18 are not obvious in light of Hong et al. Applicant submits that the above argument is equally applicable to this rejection of claims 9, 10, 22 and 24.

Claim 11, and its dependent claims 12-16, recite a semiconductor device that includes at least one memory cell. The memory cell has an active region in a substrate, a conductive plug positioned within an insulator layer and provided on the active region, an etch-stop layer, an intermediate non-conductive layer having an etched via over the plug, and at least one conductive layer in the via in electrical connection with the plug. As noted above, Hong et al. teaches away from placing a metallic layer within a via etched in a insulator layer, and so one ordinarily skilled in the art would not have been motivated to utilize the Hong et al. reference, either alone or in combination with FIG. 1 of the application.

Claims 25-32 recite a processor-based system that comprises a processing unit and a semiconductor circuit coupled to the processing unit. The semiconductor circuit

includes a substrate supporting a connection region, a conductive plug positioned within an insulator and provided on the connection region, an etch-stop layer deposited on the insulator, an intermediate non-conductive layer provided over the etch-stop layer and having an etched via over the conductive plug, and a conductive connector electrically coupled to the connection region. The conductive connector has a first conductive layer deposited in and in contact with the etched via, and the first conductive layer includes a portion in contact with the conductive plug.

As argued above, Hong et al. teaches away from the incorporation of a conductive layer within a trench or via in an insulator, and thus would have provided no motivation or suggestion to one ordinarily skilled in the art to combine Hong et al with FIG. 1.

For at least the reasons provided above, applicant believes that each of the presently pending claims is in immediate condition for allowance. Accordingly, the Examiner is respectfully requested to pass this application to issue.

Dated: May 14, 2001

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VERSION WITH MARKINGS TO SHOW CHANGES MADE

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Referring now to FIG. 8, a device constructed in accordance with the invention can be used in a memory circuit, such as a DRAM device 512, or other electronic integrated circuit, within a processor-based system 500. The processor-based system 500 may be a computer system, a process control system or any other system employing a processor and associated memory. The system 500 includes a central processing unit (CPU) 502, which may be a microprocessor. The CPU 502 communicates with the DRAM device 512, which has an array of cells 513 that include the semiconductor device 200 (or the semiconductor device 300), over a bus 516. The CPU 502 further communicates with one or more I/O devices 508, 510 over the bus 516. Although illustrated as a single bus, the bus 516 may be a series of buses and bridges commonly used in a processor-based system. Further components of the system 500 may include a read only memory (ROM) device 514 and peripheral devices such as a floppy disk drive 504, and CD-ROM drive 506. The floppy disk drive 504 and CD-ROM drive 506 communicate with the CPU 502 over the bus 516.

1. (Amended) A semiconductor structure comprising:

an insulator layer;

a conductive plug positioned within said insulator layer;

an etch-stop layer located on said insulator layer and surrounding said plug;

a non-conductive layer having an etched via at least partially over said conductive plug; and

a conductive connector formed in said via in electrical contact with said [plug] plug and including a first conductive layer deposited in and in contact with said etched via and a second conductive layer deposited over said first conductive layer, said first conductive layer including a portion in contact with said conductive plug.

9. (Amended) The semiconductor structure of claim [2] 1, wherein said first conductive layer comprises one or more materials selected from the group consisting of aluminum, copper, doped polysilicate, tantalum, tantalum nitride, titanium, titanium nitride and tungsten.

17. (Amended) The semiconductor memory device of claim 11, further comprising [an array] a plurality of said memory cells.

18. (Amended) A semiconductor device comprising:

a conductive element;

an etch-resistant layer surrounding an upper portion of said conductive element;

a non-conductive layer over said etch resistant layer and having a via over said conductive element, said via extending down to a level of said conductive element and etch resistant layer; [and]

a conductive material located in said via, wherein said conductive material contacts said conductive [element] element; and

a doped region connected to said conductive element.

26. (Amended) The processor-based system of claim 25, wherein said [conducting] conductive connector further comprises a second conductive layer deposited over said first conductive [layer, a semiconductor die being electrically connected to said conductive connector] layer.

New claim 39 has been added.